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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/753,524 | 01/09/2004 | Shunpei Yamazaki | 07977-218003 / US3531/361 | 7877 |

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| EXAMINER | |
|---|---|
| MONDT, JOHANNES P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/753,524 | YAMAZAKI ET AL. |
| | Examiner | Art Unit |
| | Johannes P. Mondt | 2826 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *1/9/04 (Filing & Preliminary Amendment)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/9/4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This office action is in response to the filing of this Divisional Application with Preliminary Amendment filed January 9, 2004.

### *Information Disclosure Statement*

The examiner has considered the items listed on the Information Disclosure Statement filed January 9, 2004. A signed copy of the Substitute Form PTO-1449 is enclosed with this office action.

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. The term "high" in ***claim 21***, and through dependence in ***claims 22-25*** is a relative term which renders the claim indefinite. The term "high" in "high resolution TEM" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Nor has Applicant provided any quantitative measure by which the image from HRTEM of his invention distinguishes from the prior art: the occurrence of spaces identified by the Specification as due to dangling bonds, between the crystal grain edges of otherwise abutting crystal grains appears, in light of the Specification, to be what the invention avoids, but in what measure is entirely unclear and is left entirely unspecified. The occurrence of dangling bonds per unit surface area of the grain boundaries in the polycrystal in the invention has not been quantified other than the discussion of Figures 17A-B pertaining to the

invention juxtaposed with Figures 17C-D characterizing the prior art. Yet the resolution at which a specific quantitative statement on the number of dangling bonds per surface area of grain boundary is made to distinguish the invention from the prior art is critical for any definiteness of the claim language. Yet the Specification does not provide any quantitative measure in this regard. For instance, Applicant merely states that in the prior art there are "many traps" (par. [0068]) while in the invention "lattice defects such as unpaired (dangling) bond are not formed ([0066]). This characterization of the crucial distinction between the invention and the prior art falls far short of being definite.

3. ***Claims 21-25*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the limitation that "lattices are continuously connected to each other *at grain boundary* of said semiconductor film" is deficient as a definite statement at least due to the absence of a particle in the underscored portion. The deficiency noted here augments the indefiniteness noted above because the claim language completely fails to quantify the needed number of grain boundaries at which lattices are "continuously connected", both in the crystalline silicon film as a whole as well as in the form of a fraction of all grain boundaries in said crystalline silicon film.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. ***Claims 21, 23 and 25*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al (5,582,640) in view of Kurihara et al (JP 08-211367 A). For convenience reference is made to the US Patent to Kurihara et al (US 5,854,627) of which aforementioned Japanese Patent with Document Identifier JP08-211367 A is the Foreign Priority Document.

N.B.: The following rejection is provided subject to the rejection as included overleaf under 35 U.S.C. 112, second paragraph and to the best understanding of the examiner.

*Okada et al teach* (27$^{th}$ Embodiment, col. 63, l. 22 – col. 64, l. 53) a thin film transistor comprising a semiconductor film 905 provided over a substrate 901/902 and comprising source and drain regions (n+ regions in Figure 92(f) connected to source and drain electrodes 909 and 910) and a channel formation region provided between source region and drain region (inherently, a channel region spans between source and drain); and a gate electrode 907 provided adjacent to said channel formation region with a gate insulating film 906 therebetween.

*Okada et al do not necessarily teach* the limitation included in the preamble, namely of the incorporation of said thin film transistor in a personal computer, nor do Okada et al necessarily teach the limitation that the lattices in said semiconductor film are "continuously connected to each other at grain boundary (sic) of said semiconductor film according to high (indefinite) resolution TEM".

*However, it would have been obvious* to include the limitation in the preamble in view of Kurihara et al, who teach a thin film transistor comprised in a liquid crystal display in a personal computer (see title, abstract and "Industrial Field of Application", col. 1, l. 9-15, col. 1, l. 16--56) wherein the liquid crystal display is placed between a pixel electrode (ITO; Figure 9 and col. 1, l. 26-32) and a liquid crystal LC (Figure 9) between said pixel electrode and said opposite electrode, thus meeting also the further limitation defined by claim 23), and opposite electrode COM (loc.cit.) . *Motivation* to include the teaching by Kurihara et al at least derives from the obvious application of TFT-LCDs in personal computers to achieve low power consumption and high picture quality as stated by Kurihara et al (abstract); while, *furthermore, Okada et al diagnosed the channel formation region inter alia by the use of TEM (col. 64, l. 9) and found that any grain boundaries pertain to very large size grains (of the order of 1200 A; col. 64); furthermore, Okada et al state that said grain boundaries do not substantially impede the mobility of charge carriers in the thin film transistor (col. 64, l. 40-45).* It would furthermore have been obvious to make the semiconductor thin film without crystal defects observable by TEM according to the third embodiment (col. 33, l. 62 – col. 23). *Motivation* to include the teaching of the third embodiment by Okada et al thus derives from the absence of a deterioration in electron mobility due to crystal defects.

*On claim 25:* the channel length by Okada et al is in a range that substantially overlaps with the claimed range and specifically includes 0.22 μm (see Fig. 117 and col. 67, l. 27-35).

6. ***Claim 22*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al and Kurihara et al as applied to claim 21 above, and further in view of Ukai et al (4,810,060). *Although an auxiliary (and deliberate) capacitance is not necessarily taught* by the combined invention, *it would have been obvious to include* an auxiliary capacitance in the personal computer in view of *Ukai*, who, in a patent on liquid crystal display devices (title and abstract) (hence analogous art), teaches to include parallel to the liquid crystal display an auxiliary capacitance so as to increase the LCD storage capacitance (it does so by increasing the RC time) (cf. claim 9 in Ukai, i.e., col. 6, l. 23-31). *Motivation* to include the teaching by Ukai at least derives from said increased storage capacitance of the LCD.

***Double Patenting***

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. ***Claim 21*** is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 5 of U.S. Patent No. 6,380,560. Although the conflicting claims are not identical, and although claim 25 in the present

application is indefinite through the absence of a particle in front of a newly introduced noun (see above under 35 USC 112, second paragraph) to the best of the understanding by the examiner they are not patentably distinct from each other because:

Claim 5 of said patent reads in essence:

A personal computer comprising a semiconductor film provided over a single crystal silicon wafer and comprising a source region, a drain region and a channel formation region provided between said source region and said drain region; and a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, wherein said semiconductor film comprises two adjacent crystals which have a grain boundary between said adjacent crystals, wherein lattice are continuously connected to each other at substantially all of said grain boundary according to high resolution TEM.

Claim 21 of the application reads:

A personal computer comprising a semiconductor film provided over a substrate and comprising a source region, a drain region and a channel formation region provided between said source region and said drain region; and a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, wherein lattices are continuously connected to each other at grain boundary of said semiconductor film according to high resolution TEM.

Underscores highlight all of the differences in the claim language.

In this regard it is noted that said single crystal silicon wafer serves as a substrate to the semiconductor film that is provided over said single crystal silicon wafer, while in the claim of the application certainly at least one grain boundary has the property claimed in claim 5 of said patent.

9. ***Claim 23*** is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 16 of U.S. Patent No. 6,730,932 in

view of Clark (ISSN: 1350-2409). According to both claims a semiconductor film is provided over a substrate and comprises source and drain regions and a channel formation region between said source and drain regions, and a gate electrode provided adjacent said channel formation region with a gate insulating film therebetween, wherein lattices are "continuously connected to each other "at grain boundary" (sic) of said semiconductor film according to high resolution TEM" and in both claims said semiconductor film is comprised in a personal computer with or through a pixel circuit (a pixel electrode inherently implies a pixel circuit as well as an opposite electrode). Claim 16 of said patent does not contain the limitation that a liquid crystal is provided between the pixel electrode and the opposite electrode. However, it would have been obvious to include said limitation in view of Clark, who teaches thin film polysilicon insulated gate field effect transistors in active matrix liquid crystal displays (abstract and sections 1 and 2). *Motivation* to include said limitation at least derives from the long-recognized and hence obvious field of application formed by active matrix liquid crystal display technology for poly-Si TFTs.

## ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JPM
March 15, 2005

Patent Examiner:

Johannes Mondt (Art Unit: 2826)